REMARKS

This amendment is in response to the Official Action dated January 29, 2007. Claims 24-44 are currently pending in connection with the present application. Claims 24, 31, 34, 36, and 41 are independent claims. To avoid confusion between the amendment after final filed April 30, 2007, which is hereby withdrawn, and this amendment, all of the former claims (*i.e.*, claims 1, 3-18, and 20-23) have been cancelled without prejudice, and new claims 24-44 have been added.

New claims 24, 25-40, and 41-44 correspond to former claims 1, 3-18, and 20-23, filed in the Amendment of October 31, 2006. However, distinctions exist between former claim 1, 5, 10, 11, 14 and 15, and new claims 24, 27, 32, 33, 36, and 37, particularly, the phrase "*when transitioning from said normal operation mode to said test mode*" has been replaced with "*at a transition time, between said test mode and said normal mode,*" or a similar variation. Claim 31 also discloses similar subject matter. This distinction is supported by ¶¶[0014-0021 and 0073-0078] of the specification (*see* U.S. PG Pub. No. 2004/0153801). Reconsideration and allowance is requested in view of the claim amendments and the following remarks.

Summary of Examiner Interview

Applicant wishes to thank Examiner Gandhi for his time spent conducting a telephone interview with Applicant's representative Christopher M. Tobin on May 15, 2007. In the Interview, Applicant's representative indicated the desire to withdraw the amendment after final filed April 30, 2007, in favor a supplemental second amendment after final. Applicant understands that the Office would need to issue an Advisory Action after a certain amount of time, perhaps by May 18, 2007 as indicated in the Interview Summary, but nevertheless confirms that the previously filed amendment is withdrawn in favor of this amendment.

Claim Objections

Applicant submits that the new claims overcome the examiner's objections regarding informalities or duplicative material present in claims 9, 15, and 19.

35 U.S.C. § 102 Rejections

Claims 1, 2, 3, 5, and 10 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Hashizume (U.S. Patent No. 6,539,511). Claims 1-13 have been cancelled. However, Applicant traverses the rejection, with regard to any applicability to corresponding new claims 24, 25, 27, and 32

Claim 24 recites: [a] *semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:*

a scan in terminal providing an inputted scan pattern to a scan chain between said scan in terminal and a scan out terminal;

a plurality of flip-flops arranged in said scan chain so as to perform scan testing for said internal logical circuitry responsive to said scan pattern;

a scan mode terminal providing a scan mode signal for switching said internal logic circuitry between said normal operation state and a scan operation state including said test mode;

a reset means for resetting said plurality of flip-flops at a transition time between said test mode and said normal mode responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal.

With respect to the resetting step, the feature of "*...resetting said plurality of flip-flops at a transition time between said test mode and said normal mode responsive to said scan mode signal for selectively...*" claims that the resetting step resets the values within the plurality of flip-flops within the transition time (i.e., the time between the test and normal mode, and vice versa). This feature may prevent the normal mode data from shifting out during test mode operation by resetting the flip-flops during the mode switch. Similarly, it may prevent the test mode data from shifting out during normal mode operation by resetting the flip-flops during the opposite mode switch.

Hashizume discloses a semiconductor integrated circuit device supporting a boundary scan test. Figure 1B illustrates the Hashizume device, including a DC test circuit 3 that sets and resets a series of flip-flops during testmode operation based on the input provided by the TESTC input line

(column 6, lines 46-51; column 8, lines 1-4, lines 32-34). During a testmode operation, DC test circuit 3 sets the values of flip-flop boundary scan registers BSR0-BSR3, and boundary scan registers/logic circuits BLU and BLD (column 6, lines 56-61). This operation changes the output of the flip-flop boundary scan registers for the next clock cycle. However, **since these registers are flip-flops, the scan registers will continue to output their prior results until the next clock cycle.** Therefore, it is still possible to read the flip-flop registers until one cycle after providing testmode data. Therefore, Hashizume does not prohibit the reading of normal mode data **while** providing testmode data.

With respect to claim 24, Applicant submits the Hashizume fails to teach or suggest, at least, "*...resetting said plurality of flip-flops at a transition time between said test mode and said normal mode responsive to said scan mode signal...*" As discussed above, Hashizume only teaches the DC test control circuit 3 set/resets the flip-flops during the TESTMODE, by loading the flip-flops with data from TESTC (Hashizume: column 6, lines 46-51; column 8, lines 32-34). Hashizume does not reset flip-flops BSR0-BSR3, BLU and BLD during the transition time between the test mode and normal mode, and thereby does not prevent the reading of normal mode data until one cycle after issuing the test signal. This one-cycle delay proves that Hashizume does not reset the flip-flops during the transition time between the test mode and normal mode, or the normal mode and test mode.

Accordingly, Hashizume fails to teach or suggest various features of independent claim 24. Furthermore, claims 27 and 32 overcome Hashizume because they depend on independent claim 24.

35 U.S.C. §103 Rejections

Claims 4, 6-9, 11-23 have been rejected under 35 U.S.C. §103(a). Claims 4, 6-9, 11-23 have been cancelled. To the extent that the rejections, including combinations of Hashizume, Cavaliere et al.(U.S. Patent No. 3,961,254), Tamamura et al.(U.S. Patent No. 6,118,316), Bae et al. (KR 200101164), DeLisle et al.(U.S. Patent No. 5,283,889), apply to claims 24-44, Applicant traverses the rejections for the following reasons.

As previously described Hashizume does not disclose, teach, or suggest at least the features of "*...resetting said plurality of flip-flops at a transition time between said test mode and said normal mode responsive to said scan mode signal...*" recited in independent claim 24. Independent claims 34, 36, and 41 also include similar subject matter to claim 24, not found in Hashizume. Furthermore, dependent claims 25-30, 32, 33, 35, 37-40, and 42-44 depend on the independent claims and therefore include the features of the independent claims not found in Hashizume.

For similar reasons, Hashizume does not disclose, teach, or suggest at least the features of "*access control means for prohibiting access to said memory means during said test mode, the prohibiting being switched at a transition time between said test mode and said normal mode in accordance with a mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal,*" recited in claim 31. In particular, Hashizume does not identify the initiation of a mode change until a clock cycle after the transition. Therefore, Hashizume cannot initiate any action prior to one cycle after the mode transition.

Cavaliere discloses an LSI semiconductor device, including circuitry for testing embedded memory arrays. Cavaliere does not disclose a technique for resetting a plurality of flip-flops at a transition time between a test mode and a normal mode. While, Cavaliere discloses inhibiting access to an LSI, Cavaliere does not disclose doing so prior to a cycle after the test mode is initiated.

Tamamura discloses a semiconductor integrated circuit for generating a stabilized oscillation signal based on an input signal. Even a cursory review of Tamamura shows that Tamamura fails to disclose a technique for resetting a plurality of flip-flops at a transition time between a test mode and a normal mode.

DeLisle discloses an integrated circuit having a reset signal, but not a testing mode. DeLisle fails to disclose a technique for resetting a plurality of flip-flops at a transition time between a test mode and a normal mode.

Bae discloses a clock generating apparatus capable of generating test pulses synchronized with another clock signal. However, Bae fails to disclose a technique for prohibiting resetting a plurality of flip-flops at a transition time between a test mode and a normal mode.

Even assuming, *arguendo*, that Hashizume, Cavaliere, Tamamura, and Bae were combinable (which Applicant does not admit), Applicant submits that none of the cited references of Cavaliere, Tamamura, and Bae, either alone or in any proper combination, cure the deficiencies of Hashizume with respect to at least the previously identified features of claims 24, 31, 34, 36, and 41.

Furthermore, at least for the reason disclosed above, claims 25-30, 32, 33, 35, 37-40, and 42-44 also overcome the combination of Hashizume, Cavaliere, Tamamura, and Bae because they depend on the independent claims.

In view of the above amendment, Applicant believes the pending application is in condition for allowance. The Examiner is invited to contact the undersigned representative regarding any issues that might resolve or expedite prosecution of this application.

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Respectfully submitted,

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